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Description

Adiabatic Charging Register Circuit

BACKGROUND OF THE INVENTION

[0001] The present invention relates to an adiabatic charging register circuit, in particular, relates to such a circuit which reduces power consumption associated with a clock pulse.

[0002] Conventionally, an LSI circuit includes a large number of register circuits, fifty thousands or more circuits. Each register circuit comprises a D-flip flop (D-FF) or D-latch circuit. A register circuit having a D-FF or D-latch is exemplified here.

[0003] First, a register circuit having a D-FF is described.

[0004] A D-FF has a pair of D-latch circuits. Fig.17 shows an example of a D-latch circuit (page 677, Structure of Design of a computer, by Paterson, and Henesey, published by NikkeiBP). A D-latch circuit 70 in Fig.17 has a pair of NOR circuits 71 and 72 which are cross-connected to each other constituting a RS-FF (reset-set-flip-flop), and a pair

of AND circuits 73 and 74. It has data input terminals D, DN in differential form, a clock input terminal CK, and data output terminals Q, QN in differential form. Each of NOR circuits 71 and 72 operates as an inverter when one of the inputs of the same is in low state, and therefore, a D-latch circuit 70 in Fig.17 operates as follows.

[0005] (1) A pair of NOR circuits 71, 72 keep a previous state when a clock input terminal CK is in low state.

[0006] (2) A value of a data input terminal D is stored in a pair of NOR circuits 71, 72 when a clock input terminal CK is in high state.

[0007] A D-FF circuit 80 is constituted by using a pair of D-latch circuits 70 as shown in Fig.18, in which a first stage D-latch circuit 70A receives a clock input CK as it is, and a second stage D-latch circuit 70B receives a clock signal which is inversion by 180E of the clock input CK by an inverter 90. A D-FF circuit operates as follows.

[0008] (1) When a clock input CK becomes to high state, the first stage D-latch circuit 70A opens to accept a data D at an input terminal,

[0009] (2) When a clock input CK becomes to low state, the second stage D-latch circuit 70B opens and an input terminal D accepts an output O1 on an output terminal Q of the

first stage D-latch 70A, as an input signal D.

[0010] Fig.19 shows operational wave forms of a data D, a clock input CK, an output O1 of the first stage D-latch circuit 70A, and an output O2 of the second stage D-latch circuit 70B. As shown in Fig.19, the output O2 is switched by an input data when a clock input CK is switched from high state to low state, thus, it is an edge trigger type circuit.

[0011] Conventionally, a clock signal CK is generated by using an inverter having a CMOS circuit which has a p-channel MOSFET and an n-channel MOSFET connected in series to each other, and has rectangular wave form. A load coupled with an output of a clock signal generator is charged to power supply voltage VDD through p-channel MOSFET of an inverter when an output signal is in high state, and is discharged to ground through n-channel MOSFET of an inverter when an output signal is in low state. Therefore, the power consumption P by a clock signal is $P=CV^2f$, where f is clock frequency, V is power supply voltage, and C is sum of capacitance of wires and gate capacitance which accept a clock signal.

[0012] The capacitance of wires is lately large because of increase of semiconductor chip area of an integrated circuit reflecting a large scale integrated circuit, and therefore,

power consumption by charge/discharge of a clock signal occupies almost 50% of the total power consumption of a semiconductor chip (page 90, Technical Report of low power LSI, Nikkei Micro-device, NikkeiBP).

[0013] Further, a large number of register circuits are used for a pipeline processing in an LSI for processing moving image, and a RISC processor. In those devices, it is also known that power consumption by a clock system is almost the same as that by a logic system (page 8, Low power and high speed LSI technology, Realize Co.). That relation is independent from operation speed, but depends upon ratio occupied by a register circuit in an LSI.

SUMMARY OF THE INVENTION

[0014] It is an object, therefore, of the present invention to provide a new and improved register circuit by overcoming the disadvantages and limitations of a prior register circuit.

[0015] It is also an object of the present invention to provide a register circuit which consumes less power in a clock system.

[0016] It is further an object of the present invention to provide a register circuit in which no short-circuit current from a power source to ground directly flows.

[0017] The above and other objects are attained by an adiabatic register circuit comprising; a plurality of n-channel MOSFET transistors and a plurality of p-channel MOSFET transistors, accepting an input data, and a clock signal, and providing an output data; said clock signal being a power clock signal having a gradually rising and gradually falling waveform generated by using a charge recycle power source in which power supplied to a load is at least partially collected to said charge recycle power source; and

[0018] following inequality is satisfied;

[0019] $$\left| V_{TN} \right| + \left| V_{TP} \right| \geq VDD$$

[0020] where V_{TN} is threshold of said n-channel MOSFET transistor, V_{TP} is threshold of said p-channel MOSFET, and VDD is output voltage of said charge recycle power source.

[0021] Preferable, said register circuit comprises a pair of D-latch circuits with an input of a second D-latch circuit coupled with an output of a first D-latch circuit, a first D-latch circuit accepts a first power clock signal, and a second D-latch circuit accepts a second power clock signal which is different by 180° of the first power clock signal.

[0022] Preferably, said D-latch circuit comprises a pair of NOR

circuits with one of the inputs of each NOR circuit being coupled with an output of the other NOR circuit, and a pair of AND circuits each accepting an input data in differential form and a power clock signal, and providing an output to the other input of each of said NOR circuit.

[0023] Preferably, said register circuit includes a combination logic circuit between said pair of D-latch circuits.

[0024] Preferably, said D-latch circuit comprises a memory element having a first inverter providing an output of the D-latch circuit, a second inverter with an input coupled with an output of said first inverter, and a first transmission gate connecting an output of the second inverter to an input of the first inverter, and a second transmission gate inserted between an input terminal and an input of said first inverter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The foregoing and other objects, features, and attendant advantages of the present invention will be appreciated as the same become better understood by means of the following description and drawings wherein;

[0026] Fig.1 is a block diagram of a D-FF circuit according to the present invention,

[0027] Fig.2A is a circuit diagram of a D-latch circuit used in the

D-FF circuit in Fig.1,

[0028] Fig.2B shows a transistor circuit of a D-latch circuit in Fig.2A,

[0029] Fig.2C shows operation of a conventional CMOS inverter,

[0030] Fig.3 is a circuit diagram of a gradually rising and gradually falling waveform generator,

[0031] Fig.4 shows waveforms of a power clock used in a D-FF circuit in Fig.1,

[0032] Fig.5 shows waveforms of another power clock used in a D-FF circuit in Fig.1,

[0033] Fig.6 shows waveforms of still another power clock used in a D-FF circuit in Fig.1,

[0034] Fig.7 shows operational waveforms of a D-FF circuit in Fig.1,

[0035] Fig.8 shows simulation result of a D-FF circuit using a conventional rectangular clock,

[0036] Fig.9 shows simulation result of a D-FF circuit using the present power clock,

[0037] Fig.10 is a block diagram of a logic system having an alternate arrangement of a D-FF circuit in Fig.1 and a logic circuit,

[0038] Fig.11 is a block diagram of another logic system having an alternate arrangement of a D-latch circuit in Fig.1 and

a logic circuit,

[0039] Fig.12 is a modification of Fig.11, and shows a pair of D-latch circuits coupled directly with no logic circuit between them,

[0040] Fig.13 shows operational waveforms of a circuit of Fig.12,

[0041] Fig.14 is another embodiment of a D-latch circuit using a transmission gate,

[0042] Fig.15 shows waveforms of a power clock used in a circuit of Fig.14,

[0043] Fig.16 shows the effect of the present invention,

[0044] Fig. 17 is a prior D-latch circuit,

[0045] Fig.18 is a prior D-FF circuit, and

[0046] Fig.19 shows operational waveforms of a D-FF circuit in Fig.18.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0047] According to the present invention, a clock signal is a charge recycle type power clock generated by using a charge recycle power source, and having a gradually rising and gradually falling waveform, while a conventional clock signal use a rectangular clock signal. A register circuit using such a power clock signal has the advantage that

power consumption in a clock system is considerably reduced as compared with that of a prior art, for instance, it is reduced to 1/10 of that of a prior art. Further, when an n-channel MOSFET and a p-channel MOSFET which constitute a register circuit satisfy the following condition, no short-circuit current from a power source to ground is allowed;

[0048] $$|V_{TN}| + |V_{TP}| \geq VDD$$

[0049] where V_{TN} is threshold of an n-channel MOSFET, V_{TP} is threshold of a p-channel MOSFET, VDD is output voltage of a power source.

(FIRST EMBODIMENT)

[0050] Fig.1 is a block diagram of a D-FF circuit 20 which is a first embodiment of the present invention. The D-FF circuit 20 comprises a first stage D-latch circuit 10A, and a second stage D-latch circuit 10B. Each of the D-latch circuits 10A and 10B is shown in Fig. 2A by the reference numeral 10, which comprises a pair of NOR gates 11 and 12 conforming an RS-FF, and a pair of AND gates 13 and 14.

[0051] The circuit of Fig.2A is implemented by a CMOS including

a p-channel MOSFET and an n-channel MOSFET, as shown in Fig.2B, in which an AND circuit and a NOR circuit are implemented by three p-channel MOSFET's and three n-channel MOSFET's as shown in the figure. Thus, the structure of Fig.2A is implemented by using two sets of a circuit of Fig.2B.

[0052] Now, a short-circuit current flowing from a power source VDD to ground directly in a CMOS circuit is analyzed in accordance with Fig.2C. In an inverter having a series circuit of a p-channel MOSFET and an n-channel MOSFET between a power source VDD and a ground, a short-circuit current from a power source VDD to ground flows during transient time of an input signal. As a power clock rises and falls slowly, a short-circuit current during transient time would be larger than that of a prior art which uses a prior rectangular clock. The upper portion of Fig.2C shows the relation between an input voltage IN and an output voltage OUT, and the lower portion of Fig.2C shows the relation between an input voltage IN and a short-circuit current. The maximum short-circuit current Imax is;

$$Imax = (\beta_n/2)((VDD - |V_{TN}| - |V_{TP}|)/(1+\sqrt{\beta_n/\beta_p}))^2$$

$$VDD > |V_{TN}| + |V_{TP}|$$

[0053] Imax = 0

[0054]
$$VDD \leqq |V_{TN}| + |V_{TP}|$$

[0055] where $\beta_n = \mu_n$ Cox (W/L)

[0056] μ_n is mobility

[0057] W is channel width of a MOSFET

[0058] L is channel length of a MOSFET

[0059] Cox is oxide capacitance per unit area

[0060] Therefore, a short-circuit current from a power source to ground is zero, even if a gradually rising and gradually falling power clock is used, when

$$VDD \leqq |V_{TN}| + |V_{TP}|$$

is satisfied.

[0061] According to the present invention, a threshold value V_{TN} of an n-channel MOSFET and a threshold value V_{TP} of a p-channel MOSFET is designed high so that the following in-equality is satisfied;

[0062]

$$| V_{TN} | + | V_{TP} | \geq VDD$$

[0063] where V_{TN} is a threshold of an n-channel MOSFET used in NOR gates 11 and 12, and AND gates 13 and 14, V_{TP} is a threshold of a p-channel MOSFET used in NOR gates 11 and 12, and AND gates 13 and 14, and VDD is power source voltage. That condition allows no short-circuit current from a power source to ground of a logic gate in a D-latch circuit 10.

[0064] Further, according to the present invention, a clock input terminal PCK of a first stage D-latch circuit 10A in a D-FF 20 receives a first power clock PCK1 which is generated by a charge recycle type power source, and has wave-form which rises and falls slowly or gradually, and a clock input terminal PCK of a second stage D-latch circuit 10B in a D-FF 20 receives a second power clock PCK2 which has different phase by 180° of that of the first power clock PCK1.

[0065] The power clocks PCK1 and PCK2 may be generated by using a gradually rising and gradually falling waveform generator 30 constituted by a switched capacitor circuit as shown in Fig.3 (1999 SSDM page 444), or an LC resonance circuit (not shown). In Fig.3, T0 - T4, T0' - T4' are a transmission gate, C1 - C3 are a capacitor. A gradually

rising and gradually falling waveform generator 30 provides a pair of power clocks PCK1 and PCK2 having a gradually rising and gradually falling waveform by conducting a pair of transmission gates sequentially in the following sequence.

[0066] (T0, T0') → (T1, T1') → (T2, T2') → (T3, T3') → (T4, T4') → (T3, T3') → (T2, T2') → (T1, T1') → (T0, T0') → (T1, T1') →

[0067] Assuming that VDD=1V,

$$\left| V_{TN} \right| = \left| V_{TP} \right|$$

= 0.7V, the operation of the first stage D-latch circuit 10A and the second stage D-latch circuit 10B is shown in Fig.4. When the amplitude of the power clocks PCK1 and PCK2 is higher than 0.7V, the D-latch circuit 10A or 10B accepts an input data, and keeps the previous status when the amplitude of the power clocks PCK1 and PCK2 is lower than 0.7V.

[0068] Figs.5 and 6 show wave-forms of power clocks PCK1 and PCK2 having different duty ratio from each other.

[0069] In those figures, the period T_{FF} shows the time from data input to data outut in a D-FF circuit 20, and the period Tcombination shows the allowable delay time allowed to a combination logic circuit coupled with an output or an input of a D-FF circuit 20.

[0070] A D-FF circuit driven by power clocks PCK1 and PCK2 is called an adiabatic charging D-FF circuit, since power consumption of power clocks are not consumed but are returned to a power supply. The adiabatic charging D-FF circuit has the following features.

[0071] (1) It has cross-wired NOR gates in static operation which is stable as compared with dynamic operation. Static operation has an output equal to VDD or 0, while dynamic operation has not only an output of VDD or 0, but also an

open output which is not VDD nor 0.

[0072] (2) No data goes directly from input to output of a D-FF circuit, since a first stage D-latch 10A and a second stage D-latch 10B do not take data simultaneously.

[0073] (3) Both D-latch circuits 10A and 10B have a period of storage mode simultaneously. In that case, each D-latch circuit 10A and 10B stores data independently.

[0074] (4) The time T_{FF} is larger than T_{FF} of a prior D-FF circuit.

[0075] (5) The power consumption is less than 1/10 of that using a conventional rectangular clock signal, since power clocks PCK1 and PCK2 are used.

[0076] (6) It is compatible with a prior D-FF. In other words, a conventional D-FF circuit constituted by a CMOS circuit using a rectangular clock signal can be substituted with an adiabatic charging D-FF circuit using a charge recycle type power source.

[0077] Fig.7 shows the operation of an adiabatic charging D-FF circuit of Fig.1. It is noted that an input data D is taken when a power clock PCK1 changes from high to low, and the data thus taken is kept for a period of the PCK2 (see an output wave form O2).

[0078] Figs.8 and 9 show the simulation result using a simulation software HSPICE. Fig.8 shows the result of a conventional

D-FF 80 in Fig.18 when a conventional rectangular clock CK is used, and Fig.9 shows the result of the present D-FF 20 in Fig.1 when the present power clocks PCK1 and PCK2 are used. The power clock PCK2 is not shown since it is the same as PCK1 but different phase by 180E phase. In the simulation, it is assumed that the gate length of an n-channel MOSFET and a P-channel MOSFET is 0.25 μm, the gate width of a p-channel MOSFET is 9 μm, the gate width of an n-channel MOSFET is 6 μm, the threshold is

$$|V_{TN}| = |V_{TP}|$$

= 0.3V, the power supply voltage is VDD=0.5 V, and the period of a clock signal (PCK1, PCK2, CK) is 100 nS (f=10 MHz).

[0079] The simulation result shows that outputs of a D-FF circuit when PCK1 and PCK2 are used are the same as those when a conventional clock CK is used.

[0080] The power consumption by a D-FF circuit with a constant power supply voltage is 320 nW in both a conventional D-FF circuit using a CMOS, and the present adiabatic charging type D-FF circuit. No increase in power consumption by a short-circuit current occurs as no short-circuit current flows. The power consumption by a conventional rectangular clock signal CK is 310 nW, while the power consumption by the present power clock signals PCK1 and PCK2 is only 23 nW. Thus, the power consumption by the adiabatic power clock signals is less than 1/10 of that of a conventional clock signal.

[0081] Fig.10 shows a logic system having alternate arrangement of a D-FF circuit 20A through 20C of the D-FF circuit 20 in Fig.1, and combination logic circuit 40A through 40C. It

should be noted that the process time in a logic circuit 40A through 40C is less than said Tcombination.

(SECOND EMBODIMENT)

[0082] Fig.11 shows the second embodiment according to the present invention. The feature of Fig.11 is an alternate arrangement of a D-latch circuit 10A through 10D of the D-latch circuit in Fig.2 and a combination logic circuit 40A through 40D. No concept of the time T_{FF} exists in this embodiment, and the allowable delay time allowed to each combination logic circuit 40A through 40D is the same as the allowed time between latch circuits using a conventional rectangular clock signal.

[0083] Fig.12 is a modification of Fig.11. In Fig.12, a pair of D-latch circuits 10A and 10B are coupled directly together with no combination logic circuit between the D-latch circuits, and the operational wave forms of Fig.12 are shown in Fig.13, which is almost the same as those of Fig.7 which shows the operation of Fig.1, except that an input data I is slightly modified so that an input data I changes from high to low at time t1 when a power clock PCK1 is higher than threshold value, the wave form of the input signal I appears in an output O1.

(THIRD EMBODIMENT)

[0084] Fig.14 shows the third embodiment according to the present invention. In this embodiment, a latch circuit is comprised of a memory circuit having a pair of inverters 60A and 60B, and a transmission gate 50B, and another transmission gate 50A connected to an input side of the transmission gate 50B. Four power clocks PCK1, PCK2, PCK3 and PCK4 are used. PCK1 and PCK2 are applied to the transmission gate 50A, and have the opposite relations with each other. PCK3 and PCK4 are applied to the transmission gate 50B, and have the opposite relations with each other. PCK1 and PCK2 are shifted by 180° from PCK3 and PCK4, respectively.

[0085] Fig.15 shows wave forms of power clocks PCK1 through PCK4.

(CONSIDERATION OF A D-LATCH CIRCUIT)

[0086] Two kinds of D-latch circuits are possible, one is an RS-FF type as shown in Fig.2, and the other is a transmission gate type as shown in Fig.14.

[0087] An RS-FF type takes static operation for input and storage of a data, and operates correctly even for slow speed operation. On the other hand, a transmission gate type circuit operates dynamically, and is not suitable to very slow speed operation.

[0088] As for a number of transistors which receive a clock signal, an RS-FF type circuit has four transistors (two transistors in each AND gate), and a transmission gate type circuit has six transistors (each transmission gate has two transistors and two transistors are used for inverting a clock signal. There are two transmission gates 50A and 50B, thus, six transistors are required). Thus, an RS-FF type circuit requires less number of transistors as far as a clock signal concerns, although an RS-FF type circuit requires more number of transistors in total than a transmission gate type circuit, and therefore, power consumption in an RS-FF type is smaller (C. Svensson and D. Liu, Low Power Design Methodologies, eds. J.M. Rabaey and M. Pedram (Kluwer Academic Publisheres, 1996) Chap.3, page 37).

[0089] The choice of an RS-FF type circuit or a transmission gate type circuit as a adiabatic charging reversible logic circuit should be designed base upon an object of a circuit, considering above analysis.

(THE USE IN SUB-THRESHOLD REGION)

[0090] In a specific condition, the current adiabatic charging register circuit can operates in weak inversion region with power supply voltage lower than threshold voltage

(sub-threshold region;

$$|V_{TP}| > VDD \text{ and } |V_{TN}| > VDD$$

), like a prior CMOS circuit. It can be applied to slow speed operation LSI in sub-threshold region such as an environment sensor, or a living body sensor.

(EFFECT OF THE INVENTION)

[0091] As described above, according to an adiabatic charging register circuit of the present invention, power consumption consumed in a clock system is reduced approximately 1/10 of that of a conventional CMOS register circuit (Fig.16). Fig.16 shows that the power consumption by a clock signal and the power consumption of a logic circuit in a prior art are almost the same as each other, on the other hand, the power consumption by a clock signal in the present invention is only 1/10 of that of a prior art. Therefore, although the power consumption by a logic circuit in the present invention is the same as that of a prior art, the total power consumption including a clock system and a logic circuit in the present invention is considerably smaller than that of a prior art.

[0092] Further, the present adiabatic charging register circuit is compatible with a conventional CMOS type register circuit.

It is enough only to substitute an adiabatic charging type register circuit with a conventional CMOS type register circuit. Thus, the design of a circuit is quite simple.

[0093] From the foregoing, it should be appreciated that a new and improved adiabatic charging type register circuit has been found. It should be understood of course that the embodiments disclosed are merely illustrative and are not intended to limit the scope of the invention. Reference should be made to the appended claims, therefore, to indicate the scope of the invention.